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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,965	12/29/2003	Kaladhar Radhakrishnan	42P18282	9014

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,965	RADHAKRISHNAN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *6,11 and 13-16* is/are rejected.

7)☒ Claim(s) *7-10,12,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed July 10, 2006. The Examiner acknowledges the amendments to Claims 1 and 3. Claims 1-18 remain pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references have been relied upon for the rejections hereinbelow:

Fujiyama et al. (US 7,023,685 B2) Rogren (US 5,625,228)

Neal et al. (US 5,946,470) Agatstein et al. (US 5,621,245)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 6, 11, 13, 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujiyama et al. [*Examiner's Note*: Claims 6 and 15 claim an IC housed by an IC package, wherein the IC is coupled to the IC package. Fujiyama et al. discloses a processor (CPU) that is referred to only as an "IC" 1 (Figs. 1 and 2; col.5: 42-43). The Examiner takes the position that the above-cited claimed structure is, in fact, **the**

fundamental structure of a processor and considers that what is shown in Fujiyama et al. is only the package alone, the IC die mounted thereto not being shown since it does not play a role in the disclosed interconnection structure. Two additional references disclosing a processor comprising the fundamental structure of an IC die housed by an IC package, wherein the IC die is coupled to a surface of the IC package, are cited by the Examiner as evidence that enables the processor structure in Fujiyama et al., as required by the Applicant's Claims 6 and 15, in accordance with the practice of multiple reference 35 USC § 102 rejections to be found in MPEP § 2131.01, part I].

As to Claim 6, Fujiyama et al. discloses an IC package 1 of 478 pins, referred to as an "IC" (Fig. 1; col.5: 38-46), for connection to a socket 3 (Fig. 6) wherein the IC package 1 is a processor but the IC coupled to the first side is present as part of the processor structure but not shown[††], since it is the pins 2 of the IC pin grid array (PGA) package 1, and not the IC die coupled to the package 1, that are among the critical elements in the invention disclosure of Fujiyama et al. (Fig. 1; col.5: 38-46); and a capacitor 31 attached to a second side of the IC package 1 underneath the IC (Figs. 6 and 7; col.7: 59-col.8: 4), the capacitor 31 having openings 11A, 12, 18 (larger diameter than that of pins 2; col.8: 5-8, 11-14 and 16-18), 13 and 19 (smaller diameter than that of pins 2; col.8: 9-11 and 18-19) to enable pins 2 from the IC package 1 to pass through (Fig. 7; col.8: 5-19).

[††]*Examiner's Note*: PGA processors as disclosed in Fujiyama et al. typically comprise an IC die coupled to a first side of an IC package substrate, which substrate often has a pin grid array for removable connection to a socket, said typical PGA processor structure evidenced

by, e.g.: (i) Neal et al. in Fig. 2: the typical processor comprises IC die 140 coupled to a central portion of the first side of package 105 (col.3: 67-col.4: 2) and pins 120 for connection to a motherboard, and in the embodiment of Fig. 10, the pins 836 of processor package 820 are connected to a socket 810; and (ii) Agatstein et al. in Figs. 1 and 2: the typical processor comprises IC die 12 coupled to a central portion of the first side of IC package 10 (col.2: 61-63) and pins 14 for connection to an unspecified higher level of packaging (typically a socket or board, as in Neal et al. and Fujiyama et al.).

As to Claim 11, Fujiyama et al. further discloses a socket 3 (Fig. 6; col.7: 59-62).

As to Claim 13, Fujiyama et al. further discloses the socket 3 is shaped to accommodate the capacitor 31 attached to the IC package 1 (Fig. 6; col.7: 59-62).

As to Claim 15, Fujiyama et al. discloses a method comprising: providing a capacitor 31 with a plurality of openings 12; providing an integrated circuit (IC), not shown, housed by an IC package 1[††]; passing pins 2 from the IC package 1 through the openings 32 formed in the capacitor 31 (col.7: 59-65); positioning the capacitor on a backside of the IC package 1 directly underneath the IC (Fig. 6); electrically connecting and attaching conductive terminals 33 between the capacitor 31 and the IC package 1 (col.7: 64-67).

[††]*Examiner's Note*: PGA processors as disclosed in Fujiyama et al. typically comprise an IC die housed by an IC package substrate, which substrate often has a pin grid array for removable connection to a socket, said typical PGA processor structure evidenced by, e.g.: (i) Neal et al. in Fig. 2: the typical processor comprises IC die 40 housed by IC package 105 wherein, IC die 140 is coupled to a central portion of the first side of package 105 (col.3: 67-col.4: 2)

and pins 120 for connection to a motherboard, and in the embodiment of Fig. 10, the pins 836 of processor package 820 are connected to a socket 810; and (ii) Agatstein et al. in Figs. 1 and 2: the typical processor comprises IC die 12 housed by IC package 10, wherein IC die 12 coupled to a central portion of the first side of IC package 10 (col.2: 61-63) and pins 14 for connection to an unspecified higher level of packaging (typically a socket or board, as in Neal et al. and Fujiyama et al.).

As to Claim 16, Fujiyama et al. further discloses electrically connecting the IC package 1 to a socket 3 (Fig. 6).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiyama et al. in view of Agatstein et al. and Rogren.

I. Fujiyama et al. discloses a processor comprising an integrated circuit, not shown, coupled to a first side of IC package 1, as evidenced by the typical processor structures of Neal et al. and Agatstein et al. but does not teach the type of IC.

II. Agatstein et al. in particular further discloses that the processor comprises an IC package 10 having an IC die (chip) 12 mounted thereon (col.2: 57-65), wherein the IC die 12 is embodied in a form of a VLSI (col.1: 28-39), which is a semiconductor die, and Rogren provides another example of a processor comprising an IC package with an IC embodied as a semiconductor die 18 coupled thereto (Figs. 1 and 2; col.44-47; col.5: 15-18).

III. Since Fujiyama et al., Agatstein et al. and Rogren are in the same field of electronics packaging including fabricating microprocessor devices, then the use of a **semiconductor** die for fabricating the many p-n junction integrated processor circuits on said die mounted on an IC package, as taught by Agatstein et al. (in the form of a VLSI) and Rogren, would have been readily recognized in the pertinent processor fabricating art of Fujiyama et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to embody the IC in Fujiyama et al. in the form of a semiconductor die, such as a VLSI, as taught by Agatstein et al. and a semiconductor die as taught by Rogren in order to fabricate the CPU in Fujiyama et al. with enhanced

processing power, as is old and well-known to be desirable in the processor packaging art, as taught by Agatstein et al. and Rogren.

Allowable Subject Matter

8. Claims 1-5 have been allowed.

9. Claims 7-10, 12, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 1-2, patentability resides in the combination of *a plurality of first conductive layers and a plurality of second conductive layers interleaved with the first conductive layers*, in further combination with the other limitations of base Claim 1. *Examiner's Note*: Regarding Claims 1 and 17, Fujiyama et al. discloses the claimed limitation that openings 32--i.e., at least some of the openings 32, specifically, openings 12 and 18--are formed such that they maintain a distance between the edge of the opening and the pins 2 (Fig. 7; col.8: 5-8). However, Fujiyama et al. teaches that the capacitor sheet comprises a plurality of first conductive layers (i.e., two conductive layers: positive conductive "sheets" 17 and 35) interleaved with only one second conductive layer (negative conductive "sheet" 11), as shown in the embodiment of Fig. 9 (col.8: 42-col.9: 8), thus forming capacitor elements 21 and 37 in sheet capacitor 31.

As to Claims 3-5, patentability resides in the limitation wherein *the openings are arranged to coincide with* ***at least four pins from the IC package that are located directly underneath a semiconductor die***, in combination with the other limitations of base Claim 3.

As to Claim 7, patentability resides in the limitation wherein *the openings are arranged to coincide with* ***at least four pins from the IC package that are located directly underneath the integrated circuit***, in combination with the other limitations of the claim.

As to Claims 8-9, patentability resides in the combination of *a plurality of first conductive layers coupled to a first node in the integrated circuit and a plurality of second conductive layers interleaved with the first conductive layers*, in further combination with the other limitations of the broader claim, Claim 8. *Examiner's Note*: Fujiyama et al. teaches that the capacitor sheet comprises a plurality of first conductive layers (i.e., two conductive layers: positive conductive "sheets" 17 and 35), inherently coupled to a first node in the IC circuit that provides the functionality of the processor, said plurality of first conductive layers interleaved with only one second conductive layer (negative conductive "sheet" 11), as shown in the embodiment of Fig. 9 (col.8: 42-col.9: 8), thus forming capacitor elements 21 and 37 in sheet capacitor 31.

As to Claim 10, patentability resides in the limitation wherein ***each of the openings*** *formed in the capacitor has a diameter which is greater than a diameter of* ***each pin*** *from the IC package such that a defined distance is maintained between an*

edge of each respective opening and ***each*** ***respective pin***, in combination with the other limitations of the claim.

As to Claim 12, patentability resides in the limitation wherein *the socket is a full-grid socket that is capable of receiving power and ground pins located on a backside of the package* ***under a die shadow***, in combination with the other limitations of the claim.

As to Claims 17-18, patentability resides in the combination of *a plurality of first conductive layers and a plurality of second conductive layers interleaved with the first conductive layers*, in further combination with the other limitations of broader Claim 17. *Examiner's Note*: Fujiyama et al. teaches that the capacitor sheet comprises a plurality of first conductive layers (i.e., two conductive layers: positive conductive "sheets" 17 and 35) interleaved with only one second conductive layer (negative conductive "sheet" 11), as shown in the embodiment of Fig. 9 (col.8: 42-col.9: 8), thus forming capacitor elements 21 and 37 in sheet capacitor 31.

Response to Arguments

11. Applicant's arguments with respect to Claims 1, 2, 4 and 5 have been considered but are moot in view of the new ground(s) of rejection.

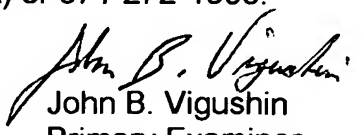
12. The above-cited new grounds of rejection includes withdrawal of the indication of allowability for Claims 6-18 from the previous Office Action of May 09, 2006 and therefore the present Office Action is made NON-FINAL.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad, can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
September 20, 2006